REMARKS

Initial Remarks:

Applicant initially notes with appreciation, the Examiner's indication in the Office Action that Claims 20-39 are allowable. In accordance with the Office Action, independent Claim 1 and dependent Claims 2 and 6 stand rejected 35 U.S.C. §102(b) and Claims 3-5 have been objected to by the Examiner. Reconsideration in view of the foregoing amendments and following remarks is respectfully requested.

Objections to the Specification:

Objection to term "amorphous hardware element":

At the end of paragraph 2 of the Office Action, the Examiner requires clarification of the term "amorphous hardware gate". The term "amorphous hardware gate" does not appear in the application, and therefore, Applicant assumes the Examiner intended to refer to the term "amorphous hardware element". Applicant respectfully submits the term "amorphous hardware element" as defined and used in the application is sufficiently precise and clear to those skilled in the art and no further clarification is necessary.

In this regard, Applicant is entitled to be his own lexicographer (see e.g., Beachcombers, Int'l v. Wildewood Creative Products, Inc., 31 F.3d 1154, 1158 (Fed. Cir. 1994) in which the Federal Circuit notes "As we have repeatedly said, a patentee can be his own lexicographer provided the patentee's definition, to the extent it differs from the conventional definition, is clearly set forth in the specification."), and accordingly, Applicant has defined in the text of the application what the term "amorphous hardware element" means within the context of the application. More specifically, Applicant states in paragraph 0036 on pages 9-10 of the Application: "As used herein, an amorphous hardware element can be any group of configurable hardware structures that can be defined to perform a particular function. Such configurable hardware structures can be gates, transistors, and/or blocks." Thereafter, in paragraph 0036 on page 10 of the Application, Applicant further clarifies an example of an amorphous hardware element, stating: "As one example, an amorphous hardware element can be an FPGA, some portion of an FPGA, or multiple FPGAs. Thus, for example, a single field programmable gate

array can include a number of amorphous hardware elements." Thus, as used in the Application, the term "amorphous hardware element" includes field programmable gate arrays (FPGAs) and is consistent with the understanding of the term employed by the Examiner for purposes of examination.

Objections to incorporation of publications by reference:

In paragraphs 3-7 of the Office Action, the Examiner objects to the incorporation by reference of a number of publications. Without admitting or denying that such material is essential, in order to advance prosecution the Application has been amended to include the relevant portions of a number of the references as Appendix A to the Application and the Application has been otherwise amended to reference Appendix A. Applicant believes that such amendment complies with the Examiner's requirement. Further, the undersigned practitioner hereby declares that, based on information and belief, the material now included in Appendix A consists of the same material incorporated by reference in the application. However, in the event that the Examiner concludes that further correction is required, Applicant respectfully requests the opportunity to comply.

Rejections under 35 U.S.C. §102(b):

In the Office Action, the Examiner rejected independent Claim 1 contending that Claim 1 is anticipated by United States Patent No. 6,057,679 to Slizynski et al. (hereafter Slizynski). Applicant respectfully disagrees and requests that such rejection be withdrawn and that Claim 1 and all claims depending directly or indirectly therefrom be allowed. In this regard, Slizynski does not disclose or reasonably suggest a system for computing seismic images having two or more processing pipelines configured within an amorphous hardware element with the processing pipelines being operable to independently update two or more seismic image points.

More particularly, Claim 1 is directed to an amorphous computing system for computing seismic images, the system comprising a first amorphous hardware element and a computer processor communicably coupled to the amorphous hardware element and to a computer readable medium. The computer readable medium includes instructions executable by the computer processor to define a first plurality of hardware gates within the amorphous hardware element to form a first processing pipeline, wherein the first processing pipeline is operable to update a first

seismic image point, and to define a second plurality of hardware gates within the amorphous hardware element to form a second processing pipeline, wherein the second processing pipeline is operable to update a second seismic image point independent of the first processing pipeline.

In contrast with the foregoing inventive combination of features, Slizynski discloses a general purpose integrated circuit tester having analog and digital channels 18, 20 between an amorphous logic circuit (ALC) 30 and a device under test (DUT) 12. (See Fig. 1 of Slizynski). Slizynski discloses that during a test of the DUT 12, the analog or digital channels 18, 20 sample output signals from the DUT 12 and send waveform data sequences they produce to terminals 28 of the ALC 30, and the ALC 30 is programmed to analyze the waveform data sequences to determine characteristics of the DUT 12 output signals. (See col. 4, lines 9-19 Slizynski). Thus, the analog and digital channels 18, 20 are merely conduits between the DUT 12 and ALC 30 and do not serve as independently operable processing pipelines within the ALC 30 to analyze output signals from the DUT 12. Furthermore, there is no mention in Slizynski that the host computer 22 programs the ALC 30 to include multiple, independently operable pipelines for processing the waveforms channeled thereto from the device under test 12 by the analog or digital channels 18, 20. Additionally, there is no mention or suggestion in Slizynski that the DUT 12 or the output signals from the DUT relate in any way to seismic image points.

In view of the aforementioned distinctions, Claim 1 is not anticipated by Slizynski and, therefore Claim 1 and all claims depending directly or indirectly there from are in condition for allowance.

Conclusion:

Applicant believes that the Application and all pending claims thereof are in condition for allowance and such disposition is respectfully requested. In the event that a telephone conversation would further prosecution and/or expedite allowance, the Examiner is invited to contact the undersigned.

Respectfully submitted,

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